Wafer Inspection as Alternative Approach to Mask Defect Qualification

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ABSTRACT

Defect inspection is one of the major challenges in the manufacturing process of photomasks. The absence of any printing defect on patterned mask is an ultimate requirement for the mask shop, and an increasing effort is spent in order to detect and subsequently eliminate these defects. Current DUV inspection tools use wavelengths five times or more larger than the critical defect size on advanced photomasks. This makes the inspectability of high-end mask patterns (including strong OPC and small SRAF's) and sufficient defect sensitivity a real challenge. The paper evaluates the feasibility of inspecting the printed wafer as an alternative way for the high-sensitivity defect inspection of photomasks. Defects originating in the mask can efficiently be filtered as repeated defects in the various dies on wafer. Using a programmed-defect mask of 65-nm technology, a reliable detection of the printing defects was achieved with an optimized inspection process. These defects could successfully be traced back to the photomask in a semi-automated process in order to enable a following repair step. This study shows that wafer inspection is able to provide a full defect qualification of advanced photomasks with the specific advantage of assessing the actual printability of arbitrary defects.

Keywords: mask inspection, defect inspection, photomask, defects, wafer inspection, alternative

1. INTRODUCTION

During the fabrication of integrated circuits, a set of many photomasks is used for the definition of the chip layout. This mask set comprises a wide range of different technologies and requirements going from critical layers with the most tiny patterns and strong OPC to less-stringent metal layers in the higher levels. Their common requirement is that every mask needs to be free of printing defects since every defect on the mask is replicated hundreds of times on the wafer and may lead to the failure of the respective chips. Thus, high attention is paid to the defect inspection of photomasks to assure a safe capture of the critical defects.

Obviously, the critical layers of a mask set are the most difficult to qualify for defects. They are characterized by the smallest features and usually include strong optical proximity correction (OPC) and extremely small sub-resolution assist features (SRAF) approaching the wafer size of the printed pattern. The size of critical defects is scaled accordingly. As an example, the minimum feature size on mask to be controlled for defects is 119 nm at a critical defect size of 52 nm for the 65-nm technology which will be again cut by half towards the 32-nm node.[1] Increasing efforts are required to ensure a reliable defect qualification of the masks, and the trend is already reached today that the metrology and qualification cost more money than the actual manufacturing.

The common approach to defect inspection of photomasks is the direct optical imaging of the mask pattern under DUV illumination and the search of weak deviations in comparison to an identical pattern copy (die-to-die) or a modeled reference (die-to-database) by sophisticated algorithms. Commercially available tools use an illumination with 257 nm or

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longer wavelengths and have a fixed optics, i. e. the inspection is non-actinic and does not consider the image transfer behaviour in the exposure tool. Nevertheless, this leads to sufficient defect detection for current technologies though systematic failures for certain defect types have been reported.[2,3]

In general, the question can be raised how far the defect sensitivity can be improved using the current approach. The critical defect size for the 65-nm technology is only 20 % of the inspection wavelength with an even more unfavourable balance in the future. Phase defects may be subject to an underestimation of their impact on the printed image if assessed with non-actinic illumination. A reduction of the inspection wavelength to 193 nm certainly will improve the defect sensitivity and avoid non-actinic artefacts for 193-nm lithography masks. Activities of such tool development have been reported recently.[4] Potential alternatives include an inspection of the aerial image (using both exposure wavelength and correct optical settings), inspection of the printed pattern on wafer or e-beam based inspection technologies.

The key questions which need to be addressed by any inspection technology are listed in the following:

- inspectability of advanced mask patterns (including OPC and SRAF's)
- sensitivity to critical defects of various origin (pattern defects, phase defects, particles, contamination)
- comparison to established methodology
- integration into existing infrastructure
- commercial viability on a small market

Every alternative mentioned above has its specific advantage. This paper focuses on the wafer inspection and investigates the feasibility for mask defect inspection from the perspective of a mask manufacturer. Similar studies have been done earlier, e. g. by A. Poock *et al.*[5], with respect to reticle re-qualification in the IC fab. It should be mentioned that such application has different constraints for cycle time, costs and optimization of the inspection process which may result in different conclusions. Here, the proof of this concept is demonstrated in the following with a programmed-defect mask at the example of a line/space layer of the 65-nm technology. Beside the inspection performance, particular attention is paid to the integration in the mask process flow requiring the back-tracking of defects to mask for repair.

2. CONCEPT OF WAFER INSPECTION

Wafer inspection is an alternative approach to the mask defect detection with a specific advantage due to its construction. It utilizes the printed pattern on the wafer and searches for differences to a reference. Based on the mask prints, the printability of defects is intrinsically included with all effects of the lithographic imaging and resist. The concept of wafer inspection as applied to the detection of mask defects is outlined in Fig. 1.

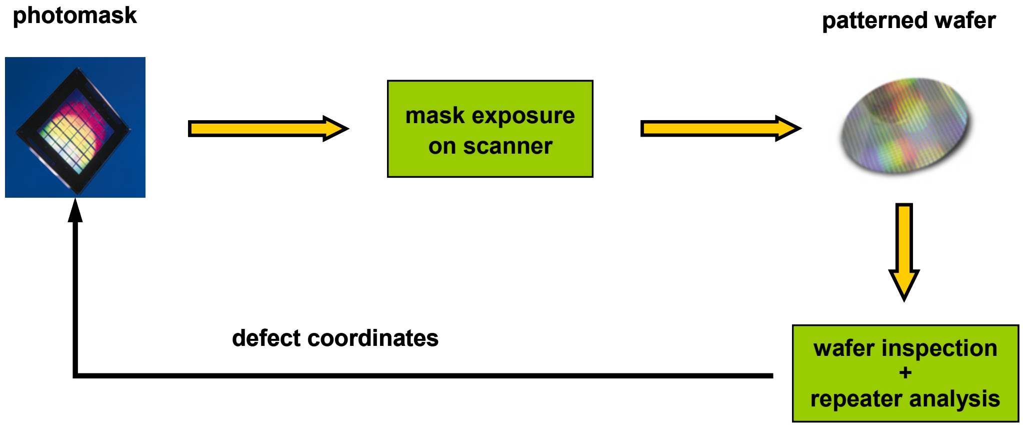


Fig. 1: Schematic view of the wafer-inspection concept for the detection of mask defects. The mask defects are indirectly detected on the printed wafer and identified as repeating defects.

In this concept, the photomask is not directly inspected for defects but sent to a lithography scanner. The mask is printed in resist on the wafer with appropriate scanner settings (NA, sigma, pupil shape, dose, defocus) similar to a product wafer. After post-exposure bake and development of the resist, this wafer is then inspected on a standard wafer-inspection tool. The mask is printed many times on the wafer, and any defect occurring on the mask is repeated in each exposure field at the same position. There might be also defects on the wafer which originate from the lithographic process but these are distributed stochastically on the wafer. A following repeater analysis is used to filter the repeating mask defects from process-related defects. Since a high-inspection sensitivity will also generate a large number of nuisance defects, the repeater analysis is also used to reject these defects. Finally, a SEM review of the identified repeaters can be performed in order to verify them as mask defect and to do a classification.

The list of repeating defects is then fed back into the mask manufacturing flow for repair. The information required is basically the defect coordinate on the photomask, the defect class and optionally a SEM image acquired during the review. The defect coordinate obtained by the wafer inspection cannot directly be used on the mask. A conversion from in-die wafer coordinates to mask coordinates needs to consider a magnification, mirroring and translation of the coordinate systems together with a multi-die layout of the exposure field, and in general can be automated. The back-tracking of wafer repeaters is successful if the actual mask defect is found within the field of view of the repair or AIMS tool.

The flow for a wafer inspection is obviously much more complex than a direct defect inspection on the photomask. However, this concept provides several advantages. First, it is a truly actinic inspection technology and includes all lithographic and resist effects since it makes use of the actual mask exposure. It thus evaluates the real printing behavior of the defects which accounts for the actual customer needs (no printing defects on the mask). Second, this implies also the same sensitivity to mask defects of different nature like pattern defects, particles, phase defects and so on because the actual impact on the printing is probed. Third, the extremely small SRAF's found on advanced photomasks do not print on the wafer and do not need to be directly inspected. Defective SRAF's on the mask are nonetheless qualified via their impact on the main-pattern printing.

Beside these technical advantages, there are further favorable aspects in respect to the infrastructure. The inspection performance basically is not dependent on the used mask type or lithography wavelength but merely driven by the technology half pitch, the critical defect size and layer type. The use of an exposure tool automatically takes the lithographic specifics into account and leaves the wafer inspection always to inspect a resist pattern on a test wafer. Furthermore, this concept utilizes no specific mask tools but relies on an established infrastructure for IC fabs with considerably more development resources. This is particularly interesting for future inspections of EUV masks making an actinic mask inspection obsolete in order to qualify a mask for defects in the multilayer.

3. EXPERIMENTAL CONDITIONS

The feasibility study was carried out using an attenuated phase-shift mask (EPSM) of the 65-nm technology. Programmed defects were distributed in a nested line/space pattern both in dark and clear tone including oversized and undersized features. Programmed defects are very useful for a systematic investigation of the inspection process since a defined range of defect sizes on mask for each defect type and their exactly known positions in the layout is provided.

This defect mask was printed in resist on a bare silicon wafer with the same illumination condition and resist thickness (incl. TARC/BARC) corresponding to a product layer. Compared to a wafer with a real product stack, a bare silicon wafer provides best signal to noise ratio and a reduced number of nuisance defects since the absence of stack fluctuations result in a very homogeneous background signal.[6,7]

The inspection of the printed pattern was done on a KLA 2800 wafer inspection tool. This is a very sensitive broadband DUV/UV/VIS inspection tool with bright field option designed for a 65-nm ground rule. The inspection recipes were developed specifically for the investigated line/space layer on the test wafer in order to achieve highest sensitivity. Since mask defects, process defects and nuisance defects are captured simultaneously during an inspection run, mask defects were identified by a repeater analysis of all detections using a special automated analysis software. This repeater analysis serves as an efficient filter discarding all other defects than mask defects (same observation as in Ref. 7). All repeater defects were reviewed in a wafer SEM for confirmation, classification and measurement of the printed defect size. Thus, the information basis for the determination of the inspection sensitivity and for a comparison to the print threshold was obtained.

This defect review confirmed the ability to sensitively detect small defects in a line/space resist pattern of the 65-nm technology node down to the printing threshold. Furthermore, a line/space pattern with SRAF features was also inspected, and no issues were observed during the inspection of such mask patterns. The sub-resolution features itself do not print on the wafer and consequently, do not need to be directly assessed (unlike in the direct mask inspection). However, defects of these SRAFs were indirectly detected by their influence on the main-pattern printing. These results demonstrate the ability of wafer inspection both to inspect advanced mask patterns on the wafer and to sensitively detect mask defects.

4. DEFECT SENSITIVITY

The first step of understanding the inspection performance of mask defects is looking at the capture rate of programmed defects printed in resist on wafer. On the wafer, sixteen chips were used in this study for inspection, i. e. each programmed defect can be detected with sixteen counts at maximum. There will be less counts for a capture rate below 100%. Contrary to a direct inspection of the photomask, a safe detection of a defect in the wafer inspection does not require a capture rate of 100%. Depending on the repeater threshold set for identification of a mask defect (usually a total of three repeaters for all inspected wafer chips), mask defects can safely be detected with a small capture rate in the wafer inspection.

The capture success of the mask defects obviously depends strongly on their appearance in the resist pattern. First of all, the defect size in the printed pattern determines the amount of scattered light which can be distinguished by the inspection tool, in contrast to the defect size on the mask. This includes a different printability of defects in different mask patterns described by the mask-error enhancement factor (MEEF).[5] Therefore, the sensitivity of the wafer inspection process should be given in terms of the physical defect size as measured in the actual wafer pattern. Second, the defect sensitivity depends on the light scattering characteristics of the defects which are influenced by the defect type and smoothing due to resist diffusion.

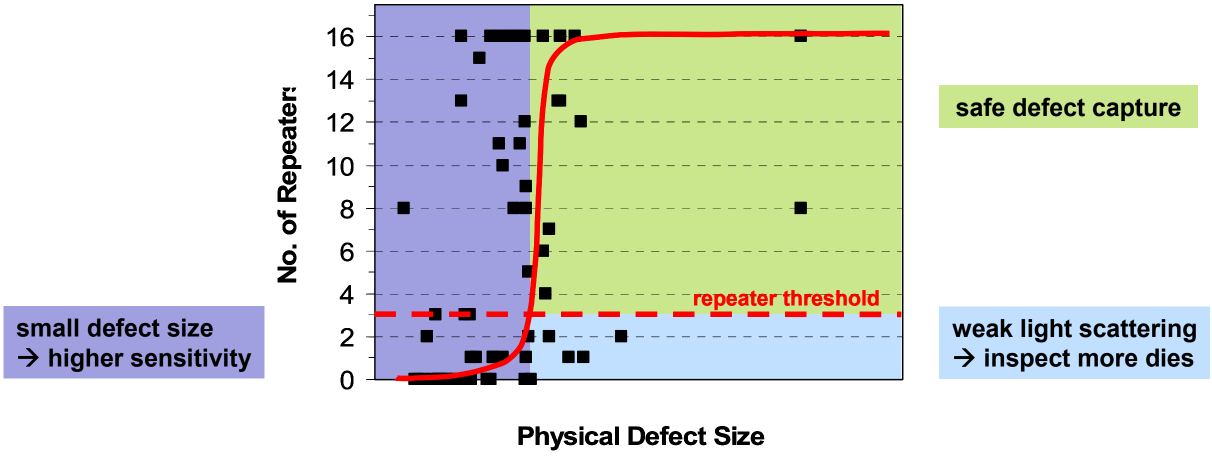


Fig. 2: Capture rate of programmed defects with the KLA 2800 wafer inspection tool in resist on a bare Si wafer. Three different regions with respect to the defect capture can be identified (see text for details).

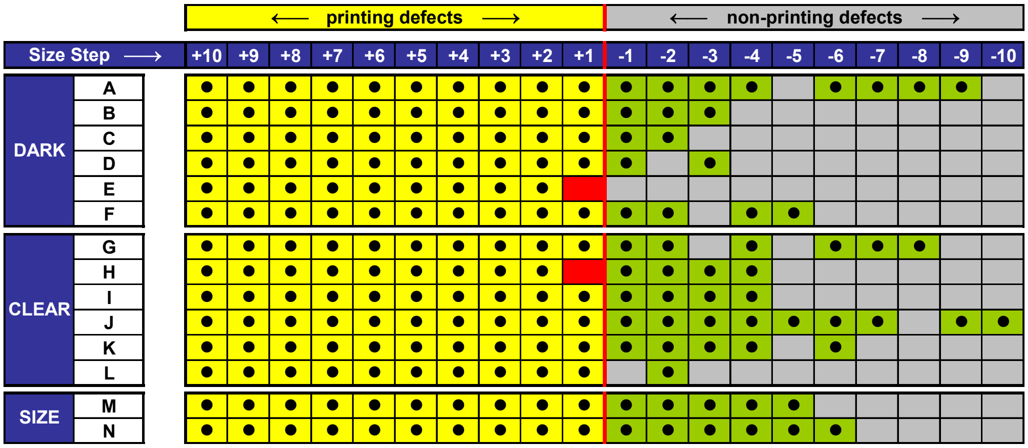
The results for the developed inspection process are shown in Fig. 2. A line/space pattern with programmed defects was inspected on test wafers (resist on bare silicon) with a KLA 2800 wafer inspection tool. For each defect, the number of detections in the sixteen inspected wafer chips was counted and plotted against the measure defect size. A minimum count of three detections is required by the repeater analysis for identification as mask defect (dashed line). All defect types of this study (both dark and clear defects) are plotted at the same time since there is a similar fundamental characteristic of the capture rate. This fundamental characteristic is indicated by the solid line as a guide to the eye.

The capture rate exhibits a sharp decrease at a certain defect size on the wafer. This detection limit for the defect size does weakly depend only on the defect type for the developed recipe. Larger defects are captured in every inspected wafer chip with a few exceptions. This region with defects above the detection limit of the inspection process and a minimum count of the repeater threshold corresponds to defects with safe capture (green area). However, there are some weak light scatterers (light blue area). Although these defects might have a size well above the detection limit, their appearance on wafer makes them hard to detect. Nevertheless, defects in this region can be detected by inspecting a higher number of wafer chips since this will eventually lift their number of counts above the fix repeater threshold. Last, defects smaller than the detection limit of the inspection process, are generally not visible. In this region of small defects (dark blue area), the sensitivity is not reliable for a safe defect detection even if the plot shows several defects with counts above the repeater threshold. Defects in this region can generally be accessed with an improved inspection process aiming in the detection of smaller mask defects. The goal for a mask qualification is the detection of all printing defects which finally determines the required inspection sensitivity.

5. PERFORMANCE OF WAFER INSPECTION

This section looks in detail on the wafer inspection performance achieved for the 65-nm technology of this feasibility study. The inspection process was optimized for this purpose in order to shift the detection limit in Fig. 2 in respect to the printability limit of the defects. The inspection performance for smaller nodes was not checked in this study but from our experience there is sufficient room for improvement to meet the higher requirements, either by tool or by process.

Figure 3 shows a comparison of the defect capture for the optimized wafer inspection process in comparison to their printability. This is the most severe criterion with respect to qualification of photomasks since no printing defects are allowed. The figure is organized such that the thick red line is separating the printing from the non-printing defects for the various defect types A … N. The programmed defect size varies from positive size steps on the left side to negative

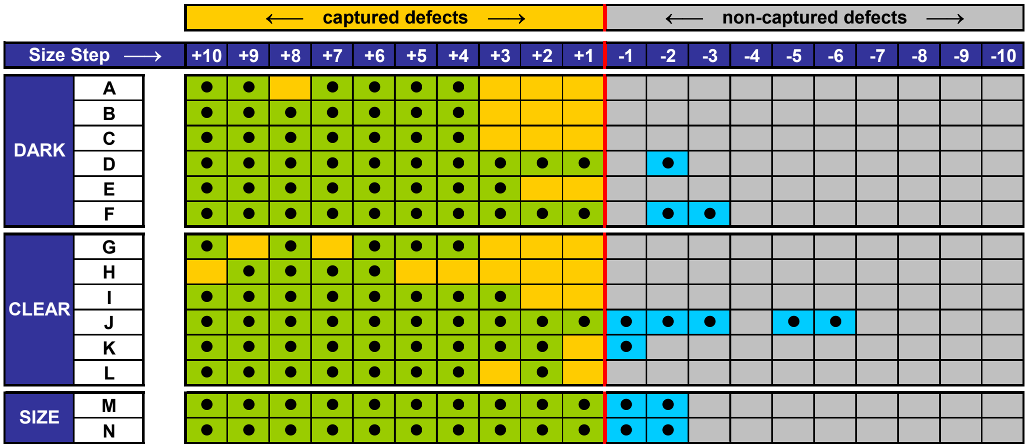


		⟵ printing defects ⟶										⟵ non-printing defects ⟶									
Size Step ⟶		+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10
DARK	A	●	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	
	B	●	●	●	●	●	●	●	●	●	●	●	●	●							
	C	●	●	●	●	●	●	●	●	●	●	●	●								
	D	●	●	●	●	●	●	●	●	●	●	●		●							
	E	●	●	●	●	●	●	●	●	●	🟥										
	F	●	●	●	●	●	●	●	●	●	●	●	●		●	●					
CLEAR	G	●	●	●	●	●	●	●	●	●	●	●	●		●		●	●	●		
	H	●	●	●	●	●	●	●	●	●	🟥	●	●	●	●						
	I	●	●	●	●	●	●	●	●	●	●	●	●	●	●						
	J	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●
	K	●	●	●	●	●	●	●	●	●	●	●	●	●	●		●				
	L	●	●	●	●	●	●	●	●	●	●		●								
SIZE	M	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●					
	N	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				

Fig. 3: Comparison of the defect capture by wafer inspection with the defect printability. An optimized inspection process on the KLA 2800 tool was applied. The dots denote captured defects, the color code marks the capture status (green – captured non-printing defect, yellow – captured printing defect, red – non-captured but printing defect).

size steps on the right side with equal steps. All defects on the left side to this line are printing according to the defect specification of the respective product layer. On the right side, these defects do not print according to the specification though there might be a minor deviation to the non-defective feature shape.

The data demonstrate that wafer inspection is capable of detecting all printing pattern defects in a line/space layer of the 65-nm technology node. A considerable number of non-printing defects (green fields) throughout the various defect types was detected going beyond the requirements for defect qualification of a photomask. Only the smallest printing defects of two defect types (E, H) were missed (red fields) though also several non-printing defects were found for one of these types. A missing defect is sometimes observed in the size series of the programmed defects but the origin of this finding is not yet understood. In conclusion, wafer inspection is a feasible alternative to inspect 65-nm patterns and to detect all printing defects if the inspection process is properly designed.



		⟵ captured defects ⟶										⟵ non-captured defects ⟶									
Size Step ⟶		+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10
DARK	A	🟩●	🟩●	🟧	🟩●	🟩●	🟩●	🟩●	🟧	🟧	🟧	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
	B	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟧	🟧	🟧	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
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	D	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	⬜	🟦●	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
	E	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟧	🟧	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
	F	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	⬜	🟦●	🟦●	⬜	⬜	⬜	⬜	⬜	⬜	⬜
CLEAR	G	🟩●	🟧	🟩●	🟧	🟩●	🟩●	🟩●	🟧	🟧	🟧	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
	H	🟧	🟩●	🟩●	🟩●	🟩●	🟧	🟧	🟧	🟧	🟧	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
	I	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟧	🟧	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
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	K	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟧	🟦●	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
	L	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟧	🟩●	🟧	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
SIZE	M	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟦●	🟦●	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜
	N	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟩●	🟦●	🟦●	⬜	⬜	⬜	⬜	⬜	⬜	⬜	⬜

Fig. 4: Comparison of the defect capture by wafer inspection and by direct mask inspection. The color code marks the capture status (green – captured by both technologies, orange – captured only by direct mask inspection, blue – captured only by wafer inspection).

In a next step, a benchmarking to the direct mask inspection as standard approach was conducted. The performance comparison of indirect wafer inspection to the direct optical mask inspection is shown in Fig. 4. A similar scheme was chosen than for the comparison to the defect printability above. This time, the programmed defects are re-arranged such that the left side to the thick red line shows all defects captured by the standard direct mask inspection and the right side the non-captured ones. The defects detected by wafer inspection are again marked by a dot.

The defect sensitivity of the wafer inspection is not as high as that of the direct mask inspection. Several of the small programmed defects are only detected by direct mask inspection (orange fields). However, for certain defect types, wafer inspection is even more sensitive and goes beyond the detections of the direct mask inspection (blue fields). This illustrates that there is no clear favorite for all purposes. Actually, an optimum inspection process for a given mask layer would have its sensitivity tuned in order to detect only the printing and none of the non-printing defects (with a slight safety margin). On one hand, missing a printing defect is a fatal error but on the other hand, every captured non-printing defect increases the effort and cycle time (classification, repair, verification).

6. BACK-TRACKING OF DEFECTS TO THE PHOTOMASK

After looking at the performance of wafer inspection, the last section deals with the integration of the wafer-inspection concept into the mask process flow. Instead of a single process step for direct mask inspection, wafer inspection requires a loop of several process steps with mask printing, wafer inspection, repeater analysis and optionally a SEM review on the wafer. The inspection result is fed back into the mask process as a list of detected defects together with their coordi-

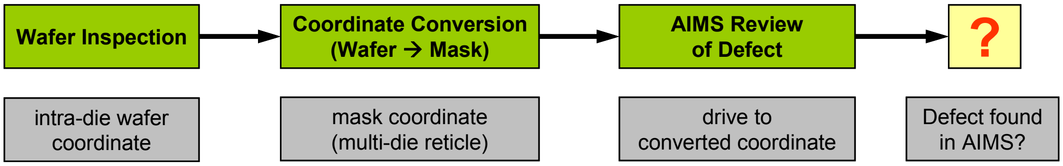

Fig. 5: Schematic flow for the back-tracking of defect detections to the mask. The back-tracking is considered to be successful if the defect is safely found within the field-of-view of the AIMS tool.

nates (inspection report) similar to the data from the direct mask inspection. This information is then used in subsequent repair or AIMS steps to drive to and work on these defects.

Beside a definition of data flow and interfaces, the technical question arises if the inspection output on wafer level can be used for a precise back-tracking of the defects to the mask. The basic question here is whether the detected defect is found in the field of view of the repair or AIMS tool. The success is mainly driven by the accuracy of the wafer-inspection output and the correct conversion algorithm from wafer to mask data. The coordinate conversion includes magnification, mirroring, translation to the mask coordinate system and the assignment of the repeater to the correct die on multi-die photomasks. The data flow is schematically shown in Fig. 5 for illustration.

The back-tracking of the defects was tested with a number of repeaters all collected during the same wafer-inspection run. The machine output was analyzed for repeaters and semi-automatically converted to mask coordinates. The test is finally considered being successful if the programmed defect appears inside the field-of-view of the AIMS tool by driving to the converted coordinate. Three representative examples of the outcome can be found in Fig. 6. The field size for AIMS measurements is 10µm × 10µm (orange frames in Fig. 6) but a somewhat larger view can be used for defect searching. If the defect cannot be observed in the window, the only opportunity is a lengthy and risky procedure of moving the mask and searching the surrounding for the defect.

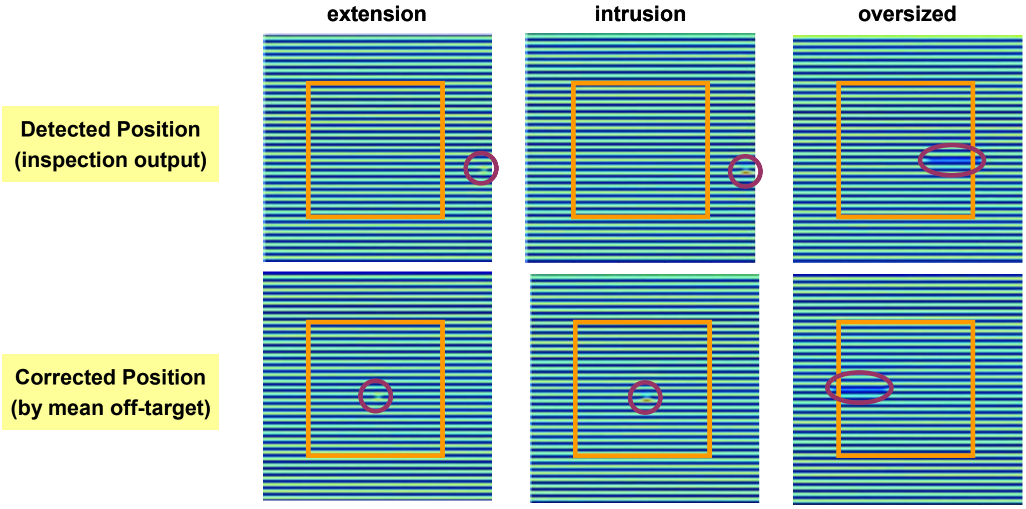

Fig. 6: Field-of-view of the AIMS tool after driving to the inspection coordinate of programmed defects (representative examples). The defects (circles) appear close to the edge of the FOV but move to the center after correction by the mean off-target. The actual measurement field is marked by the orange frame.

The upper row in Fig. 6 shows the view of the AIMS tool if driving to the converted coordinate. All defects checked appear at roughly the same position near the edge of the extended field of view. The defects were successfully found, however, in some cases they were almost outside the field. Since all defects were observed at similar positions, the target coordinates for the test were corrected by the mean displacement of all defects from the field center which is shown in the lower row. Now all defects are safely found close to the center of the field.

The origin of this displacement in the AIMS review is related to a shift of the inspection output. A comparison of the coordinates obtained from the wafer inspection tool and the defect positions in the mask layout (coordinate off-target) as shown in Fig. 7 reveals a narrow distribution of the defect off-targets (roughly 2µm on mask scale) with a relatively large translation to the target position by 7.5µm. The same translation applies to every defect of the same inspection run and is possibly introduced by the wafer alignment in the inspection tool. If this translation is corrected, the wafer inspection yields a highly accurate defect position so that the detected defects are easily found in the following repair steps.

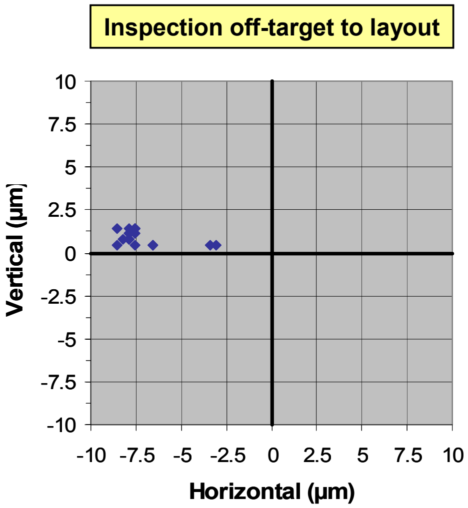

Fig. 7: Off-target of the inspection output to the position of the programmed defect in the layout (mask scale). A zero off-target means that the inspection output hits exactly the defect position. There is a global off-target of approx. 7.5µm but with a narrow distribution within the same inspection run.

7. CONCLUSIONS

This study has investigated the feasibility of wafer inspection as an alternative approach to the detection of mask defects. An advantage of wafer inspection is the actinic assessment of the mask integrity taking the actual printability on the wafer into account. Since the wafer is inspected, the inspection performance is mainly depending on the feature size of the printed features and the pattern type only, and not directly related to the nature of the defect or the mask type under investigation. This is seen as a particular advantage for the inspection of EUV masks where both pattern defects, particles and defects in the multilayer can be inspected simultaneously.

The feasibility was shown with optical lithography for programmed defects in a line/space pattern of 65-nm technology. The repeater analysis is able to filter efficiently for nuisance defects and ensures a high defect sensitivity for mask defects. With an optimized wafer inspection process, a capture of almost every printing defect was achieved in this study (only two missing defects). There were also a considerable number of detected defects beyond the printability specification. A comparison of wafer inspection to the standard direct mask inspection showed no clear advantage to either technology at the given mask ground rule in respect to the sensitivity. The repeaters can be accurately traced back to the mask and found in a subsequent repair or AIMS step if a global displacement originating in the inspection process is corrected for.

The conclusion of this feasibility study is that wafer inspection shows a great potential to be used as highly sensitive inspection approach for the detection of mask defects. It has a number of specific advantages, in particular the assessment of the real print image and of the actual printability of defects. For the 65-nm technology, slight fine tuning of the optimized wafer inspection process is necessary in order to reach the inspection capability and sensitivity for the detection of all printing defects. An extension of the wafer inspection to the defect qualification of future technology nodes seems to be possible.

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