Multi-Shaped E-Beam Technology for Mask Writing

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ABSTRACT

Photomask lithography for the 22nm technology node and beyond requires new approaches in equipment as well as mask design. Multi Shaped Beam technology (MSB) for photomask patterning using a matrix of small beamlets instead of just one shaped beam, is a very effective and evolutionary enhancement of the well established Variable Shaped Beam (VSB) technique. Its technical feasibility has been successfully demonstrated [2]. One advantage of MSB is the productivity gain over VSB with decreasing critical dimensions (CDs) and increasing levels of optical proximity correction (OPC) or for inverse lithography technology (ILT) and source mask optimization (SMO) solutions. This makes MSB an attractive alternative to VSB for photomask lithography at future technology nodes.

The present paper describes in detail the working principles and advantages of MSB over VSB for photomask applications. MSB integrates the electron optical column, x/y stage and data path into an operational electron beam lithography system. Multi e-beam mask writer specific requirements concerning the computational lithography and their implementation are outlined here. Data preparation of aggressive OPC layouts, shot count reductions over VSB, data path architecture, write time simulation and several aspects of the exposure process sequence are also discussed. Analysis results of both the MSB processing and the write time of full 32nm and 22nm node critical layer mask layouts are presented as an example.

Keywords: Photomask lithography, Multi Shaped Beam, MSB, mask write, MW, shot count reduction, electron beam lithography, computational lithography, Variable Shaped Beam, VSB

1. INTRODUCTION

Earlier publications explain in detail the working principle of the Vistec Multi Shaped Beam (MSB) technology [1] and demonstrate first lithography results on test and customer patterns [2]. The MSB working principle (see Figure 1) is appropriate for both wafer direct write and photomask write applications. Based on a common Vistec tool platform, it will be possible to configure direct write tools for wafers up to 450mm in diameter and photomask writers with a smaller square stage system. This prompted a close examination of the entire data preparation path for very different mask and direct write applications [3], [4]. Shot count reductions are clearly demonstrated with MSB technology when compared to the (single) standard shaped beam mask writer approach as shown in the later results.

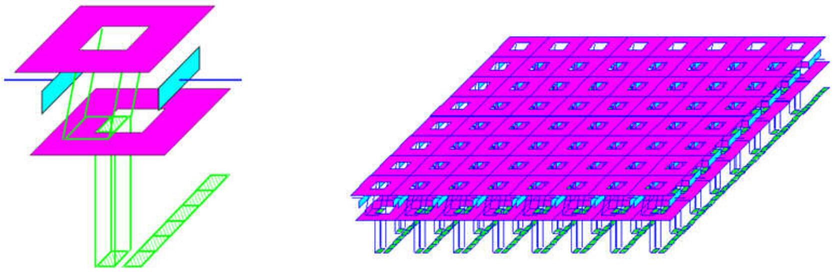


Figure 1: Schematic comparison of single variable shaped beam VSB (left) and Multi Shaped Beam MSB (right) technique

This report discusses the write time savings obtained by shot count reductions in MSB, using a set of 32nm critical mask layers, described in the following section. Additionally it provides an outlook to future 22nm technology applications.

2. METHODOLOGY OF SHOT COUNTING

To quickly extract an overview of the tool-specific fracturing results a Vistec / EQUIcon internal software tool (Shaped Beam Shot Statistics – SBSS) is used. This tool determines and analyzes the shot size distribution as a result of the layout data preparation procedure. The analyses provided by this tool represent the general layout characteristics. Fill pattern elements with relatively large shapes lead to a higher portion of big shots, while model-based layout data (OPC, ILT, SMO) lead to a large amount of smaller shots [5], [9]. The same result is observed for contact or via layers, where naturally the majority of shapes size is close to the target size of the contact holes. This methodology allows also to show in applications with curved patterns, respectively ILT patterns [5], the impact of the selected approximation quality on the numbers of shots in the different shot size classes.

3. DATA COLLECTION

3.1 Mask Layout Characteristics

The pattern data used here is a 32nm node 4:1 mask layout of a logic IC. The layers analyzed in this study were: ACTIVE (active silicon conductor layer), POLY GATE (gate poly silicon conductor layer), METAL (first metal layer) and VIA (first via layer). For each layer the main pattern (54 x 64mm²) is placed twice on the mask. Basic information on the 4 selected layers is given in Table 1

Table 1: Overview of the test data set. OASIS data volume and average local pattern density (Written Area) per layer

Layer	**Data Volume (OASIS) [GByte]**	**Pattern Density (main pattern only)**
ACTIVE	17.0	44.1%
POLY GATE	31.0	43.7%
METAL1	59.0	41.5%
VIA1	5.6	11.5%

The following investigations always describe a complete mask, i.e. the main patterns + chip frames as well as labels, fiducial marks etc., if not noted differently.

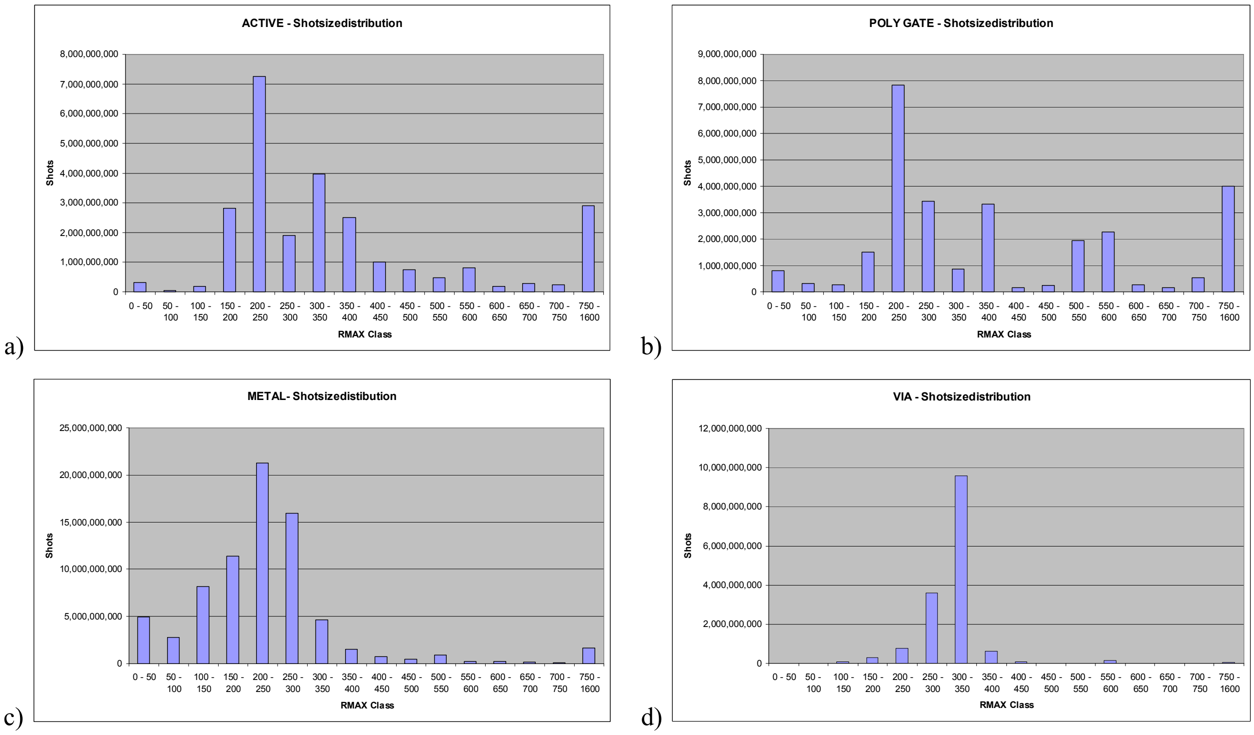


Figure 2: Shot size distribution in [shots/size class] for all main pattern; x-axis: shot size classes, y-axis: number of count a) ACTIVE layer, b) POLY GATE layer, c) METAL layer, d) VIA layer

3.2 Shot Counts of Test Data Set

Figures 2a) through d) show the shot size distribution analysis of the four examined layers from our test data set. According to the distribution graphs, classes of the longest rectangular shape (RMAX) edges are depicted on the X-axis, while the corresponding number of shots per class is plotted along the Y-axis. Figure 2d) shows the typical result of a VIA layer with via sizes in the range between 300 and 350nm while the ACTIVE layer (Figure 2a) and Poly Gate layer (Figure 2b) obviously contain a higher portion of coarse patterns and other larger (i.e. line-type) geometries.

Using the data generated via the above mentioned SBSS analyzing tool one is capable of defining an optimum characteristic of the shaped beam tool. It is obvious that particularly the maximum shape of the MSB beamlets or the single beam should be matched appropriately in order to achieve a small shot count number and thus a short write time. VSB tools with maximum shape sizes decreasing for each new tool generation down to 0.8µm [5] or respectively 0.5µm [6] are prepared for model-based layouts (OPC, ILT), however, write time disadvantages appear, if coarse layout parts, such as fill patterns, long lines etc. are processed. The combination of a standard (single) shaped beam of 1.6µm maximum shape size with a beamlet matrix in the electron-optical beam path is therefore an ideal conceptual solution for the Vistec MSB tool.

4. RESULTS

4.1 Comparison of Shot Counts and Write Times

A comprehensive layout data preparation package including proximity effect correction (PEC) is provided by EQUIcon / Vistec and available for all Vistec shaped beam writers as well as for the new MSB generation [3], [4]. Thanks to these software tools, it is possible to determine the exact number of shots to be exposed. Based on this and as described in [4], it is possible to simulate the write time in taking into account the resist sensitivity, the beam current density and, the PEC. For all layouts described in chapter 3 the corresponding values were determined.

It should be pointed out that we differentiate between standard shot (rectangle, triangle, slant) and M-shot (= multi shaped beam, MSB-shot). An M-shot is the exposure of n beamlets at the same time (flash), where each beamlet may have its own individual size, dose, and within certain limits, also its own position. Beamlets are elements of the multi shaped beam array. The MSB matrix [1], [2] may, for instance, consist of 8 x 8 beamlets (MSB64) or 16 x 16 beamlets (MSB256). Higher numbers of beamlets are taken into account for Direct Write (DW) applications [8]. In case of MSB64, the maximum beamlet size is considered to be 200 x 200nm² and in case of MSB256, this will be 100 x 100nm². Other beamlet configurations like 400 x 400nm² have been evaluated as well.

In this chapter also write time values of a single shaped beam tool using 50kV, 50A/cm² current density and a maximum shot size of 1000nm are compared with the write time simulation values of an MSB tool using 50kV, 20 A/cm² combined with different beamlet matrix configurations. In parallel to the MSB matrix, the single shaped beam with a max shape size of 1.6µm was used. The structure size criteria to preferably use single VSB can be specified and configured in order to optimize the throughput.

The METAL, VIA and ACTIVE layers are exposed on a pCAR (positive chemically amplified resist) with 10µC/cm² L/S dose (50% dose), while the POLY GATE layer has been exposed on nCAR (negative CAR) with 15µC/cm² L/S dose. Corresponding PEC functions have been applied using 250 dose classes. All applied lithography settings were reasonably proven in the first exposure results [2]. The write time results refer to double pass exposure and cover the entire mask including frame, marks, labels etc.

Table 2: Overview of shot counts and write times for each mask layer using single-VSB and MSB with several different beamlet sizes and multi-beam matrices

Tool Type	Layer	Beamlet Matrix Size	Maximum Beamlet Size [nm]	Shot / M-Shot Count [10^9]	Write Time [hh:mm]
VSB 50A/cm², 50kV	METAL	n.a.	n.a.	145	11:14
MSB 20A/cm², 50kV	METAL	64	200	22	05:23
		64	400	15	03:23
		256	100	19	05:04
VSB 50A/cm², 50kV	VIA	n.a.	n.a.	31	04:24
MSB 20A/cm², 50kV	VIA	64	200	9	04:05
		64	400	5	02:16
		256	100	9	04:04
VSB 50A/cm², 50kV	ACTIVE	n.a.	n.a.	59	05:31
MSB 20A/cm², 50kV	ACTIVE	64	200	17	04:09
		64	400	12	02:41
		256	100	16	03:58
VSB 50A/cm², 50kV	POLY GATE	n.a.	n.a.	66	08:30
MSB 20A/cm², 50kV	POLY GATE	64	200	24	07:23
		64	400	19	05:06
		256	100	23	07:12

In Table 2 one can clearly see that a significant shot count reduction can be achieved by implementing the MSB technology. This also supports the values disclosed in [3].

Using a 64 beamlet matrix of maximum 200nm beam size already leads to a shot count reduction and thus to improved throughput performance. As shown in Figures 2a) through 2d), in all layers the shot size distribution indicates that it is worth to investigate whether an additional throughput gain can be obtained by matching the maximum beamlet size, e.g. increase from 200nm to 400nm (beamlet size control). Table 2 shows the advantage of such an adaptation. Electron-optical calculations state the feasibility of a beamlet matrix with 8 x 8 elements combined with a maximum beamlet size of 400nm.

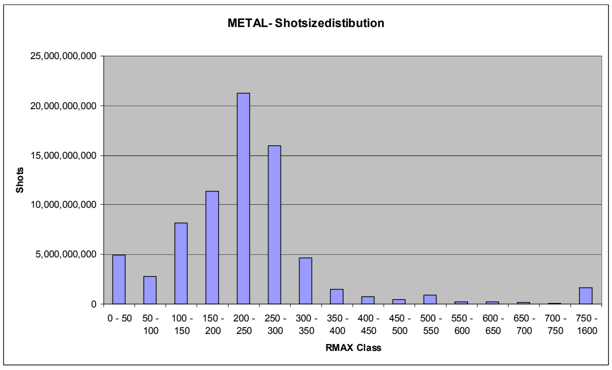
Table 2 illustrates that using 256 beamlets instead of 64 beamlets does not significantly influence the throughput improvement for the assigned 32nm node mask write patterns, as this can be already concluded from the non-matched beamlet size indicated in the results of the shot size distribution in the graphs in Figures 2a) through 2d).

In general it can be stated that the MSB technology leads to a throughput improvement for this mask set layer depending up to a factor of more than 3 versus VSB.

4.2 Outlook to 22nm Technology Node

To forecast the feasibility of the MSB technology with respect to 22nm technology, the most compact layer of the present 32nm data record (METAL) was scaled with a factor of 0.7 and then arranged as a 3 x 3 matrix on a mask. Analogously to the conditions specified under 4.1 (single shaped beam tool using 50kV, 50A/cm² with a maximum shot size of 1000nm and MSB tool using 50kV, 20 A/cm², both with double pass, resist L/S dose 20µC/cm²), the write time was determined for this jobdeck. As already explained in chapter 4.1, also in this case the single VSB (maximum 1.6µm) could be used in parallel to the MSB matrix. The shot size distribution graph in Figure 3b) shows that a beamlet size of maximum 200nm appears to be appropriate for the 22nm technology node METAL layer, while 400nm beamlet size is more suitable for the 32nm node (see Figure 3a).

a)



b)

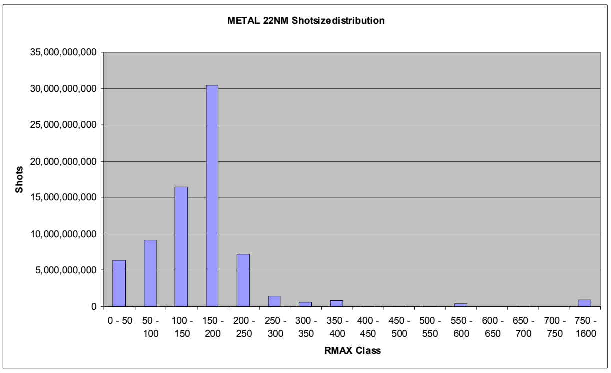


Figure 3: shot size distribution of METAL layers from different technology nodes
a) METAL 32nm node - 54 x 64mm² placed 1 x 2
b) METAL 22nm node (32nm scaled by 0.7) – 38 x 45mm² placed 3 x 3

A comparison of the VSB and MSB write times for 22nm node pattern is given in Table 3. Write time advantages are achieved for the MSB principle, despite of lower current densities. Please note that even patterns with dimensions larger than the maximum beamlet size can be exposed without any negative effects to the exposure time. This has mainly two reasons:

- Flexible selection between MSB shot and standard single beam shot (currently 1.6µm maximum shape size) which is available in parallel to the MSB matrix
- The parallel exposure of several extended structures within one Multi-shape-shot

Additional improvements are possible, if the design of non-functional elements like fill pattern is adapted to the implemented MSB matrix configuration.

Table 3: 22nm node: write time results of Metal 1 layer mask (3x3 matrix of METAL main pattern).
For VSB only results from write time estimation are available.

Tool Type	**Shot Count [10^9]**	**Write Time [hh:mm]**
VSB 50A/cm², 50kV, maximum shot size 1000nm	669	75:32
MSB 20A/cm², 50kV, 64 beamlets, maximum beamlet size 200nm	51	9:04

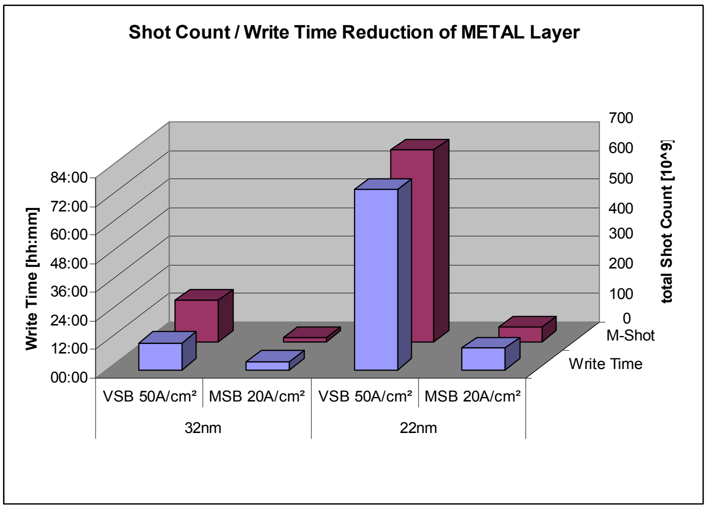


Figure 4: Comparison MSB / VSB advantage 32nm versus 22nm node of Metal 1 layer mask

Fig. 4 shows that the advantage of the MSB concept will even increase for future technology nodes compensating the increasing shot counts.

This 22nm mask write data forecast allows us to recognize the advantages of the MSB technology for ILT. Currently, the high shot counts and the related long write times are one reason preventing the introduction of idealistic ILT masks; instead approximated ILT layouts are used. Now, applying MSB technology, it becomes possible to expose ILT masks without significant losses in neither productivity nor pattern approximation.

5. CONCLUSIONS

MSB data preparation and write time simulation tools exist in first version and have already the capability to process complex pattern data. These tools present the base for further optimizations of the data path and further write time reductions. The current status has been demonstrated on a 32nm node mask set with 4 critical layers and a selected dense

22nm layer. In the case of the dedicated mask set we observed not only significant shot count reductions, but also write time reductions compared to standard VSB with 50A/cm² current density. For design of 32nm technology node patterns and more mature ones, additional throughput improvements can be best achieved with an adapted maximum beamlet size of 400nm. Using 256 beamlets instead of 64 beamlets does not have any impact on the throughput improvement for the assigned 32nm node mask patterns.

From our analysis one can conclude that the beamlet size in combination with the MSB matrix size has to be adjusted to the technology node:

- 45 / 32nm MW nodes can be best supported by 400nm maximum beamlet size and a matrix of 8 x 8 beamlets.
- Technology nodes below 32nm show optimized write times with 200nm beamlets on a matrix of 8 x 8

At 20A/cm², MSB technology allows a significant throughput improvement to be obtained relative to single shaped beam technology (50A/cm²) by using a 8 x 8 beamlet matrix. The 22nm node layer derived by pure scaling shows a write time reduction from more than 75 hours on single VSB down to about 9 hours when using MSB. This shows the extendibility of the MSB technology for future technologies and technology nodes effectively compensating the increasing shot counts to be expected. Furthermore, the advantage of the MSB concept will even increase for future technology nodes. With other words, the presented MSB technology can overcome the currently visible barriers seen by the mask write community [9].

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REFERENCES

[1] Slodowski, M., et al., "Coulomb Blur Advantage of a Multi Shaped Beam Lithography Approach", Proc. SPIE 7271, (2009)

[2] Slodowski, M., et al., "Multi Shaped Beam Proof of Lithography", Proc. SPIE 7637, 41 (2009)

[3] Weidenmueller, U., et al., "Multi Shaped Beam Data Prep", EMLC, Proc. SPIE 7545, 21 (2010)

[4] Gramss, J., et al., "Latest Results and computing performance of the ePLACE", Proc. SPIE (BACUS) 7488, 79 (2009)

[5] Kim, B.-G., et al., "Inverse lithography (ILT) mask manufacturability for full-chip Device", Proc. SPIE (BACUS) 7488, 95 (2009)

[6] Kamikubo, T., et al., "Electron-beam mask writer EBM-7000 for Hp 32-nm generation", Proc. SPIE (BACUS) 7488 ,48 (2009)

[7] Kamikubo, T., et al., "New electron optics for mask writer EBM-7000 to challenge hp 32-nm generation", Proc. SPIE (BACUS) 7122, 17 (2008)

[8] Slodowski, M., et al., "Multi-Shaped-Beam (MSB): an evolutionary approach for high throughput e-beam lithography", Proc. SPIE (BACUS) 7823, 139 (to be published) (2010)

[9] Faure, T.B., "Will Mask Writer Throughput Limit Optical Lithography?", BACUS News Editorial 26, Issue 7 (July 2010)