Mask R&D Activities at the Advanced Mask Technology Center

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ABSTRACT

The Advanced Mask Technology Center (AMTC) in Dresden is an equally-owned joint venture of Advanced Micro Devices Inc. (AMD), DuPont Photomasks, Inc. (DPI), and Infineon Technologies AG (Infineon) founded in 2002 to create a world-leading mask R&D center for both DRAM and logic applications. The AMTC's primary focus is research and development of sub-70 nm technologies. While 193 nm lithography will be used for 65 nm design rules and is probable for 45 nm design rules, solutions for sub-45 nm design rules are still being studied. Possible solutions include 193 nm immersion, 157 nm immersion, EUV, and EPL or its variants. The AMTC is actively involved in multiple collaborative projects to develop masks for advanced lithographies. This paper presents a sampling of AMTC's development activities on both conventional and EUV masks.

Intensive studies on adequate materials and their properties for the respective technology have been performed with key partners in the field. Masks have been produced and analyzed. New repair processes have been developed for the small structures of future nodes, the printing capabilities have been predicted by AIMS measurements and analyzed with printing experiments at the respective wavelengths. In this talk we will present the latest results of simulations, experiments, handling and tool qualifications performed at the AMTC or with its partners.

We will especially focus on our activities for the EUV technology and will present results on material and process development as well as on simulations for soft and hard pellicle induced distortions. For the EUV technology we will present preliminary results from our etching experiment on binary masks. First results on the performance of our new nano-machining RAVE tool will be shown.

Keywords: mask technology, RET, pellicle, etch, repair, EUV, absorber, reflectance

1. INTRODUCTION

Time to market is increasingly important in the semiconductor industry, particularly for high volume products such as DRAMs and microprocessors because these products witness sharp price reductions shortly after release. In the past, time to market was dominated by chip design and production. Recently, the proliferation of resolution enhancement technologies (RETs, examples of which are optical proximity correction – OPC – and phase shifting masks – PSMs) has increased mask design and manufacturing complexity and cycle time so that the mask is now a significant part of time to market. Thus, mask manufacturing cycle time can be a competitive advantage.

The solutions for 65 nm design rule lithography are largely set. Early in this node, solutions will combine 193 nm wavelength, moderate numerical aperture (~0.85), and phase shifting masks with OPC. Solutions for late-65 nm and 45 nm are somewhat less certain, but 193 nm immersion lithography has become a leading candidate because its hyper-NA (i.e., NA>1) offers significant resolution improvement without the expense of a wavelength change. 32 nm design rule lithography solutions are uncertain currently. Possible solutions include 193 nm immersion (with perhaps some "exotic" exposure strategies), 157 nm immersion, EUV, and EPL or its variants. To explore mask technology for these advanced lithography nodes, the AMTC is participating in multiple mask-related research projects.

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1.1. Advanced Mask Technology Center Concept

An effective approach to cycle time reduction is supply chain integration, in which development and deployment of lithography solutions are accomplished cooperatively among semiconductor and photomask partners. The AMTC in Dresden, Germany, an equally-owned joint venture of AMD, DPI, and Infineon, is a good example of this concept. The AMTC is a world-leading center for R&D and pilot production of photomasks for the most advanced lithography technologies. The AMTC's charter includes development of mask materials, processes, equipment, and IT methods for both conventional and next-generation lithographies.

In parallel with the creation of the AMTC, DuPont Photomasks established an independent state-of-the-art commercial photomask production facility, DuPont Photomasks Dresden, which is housed in the same building as the AMTC. DuPont Photomasks Dresden will produce high-end photomasks for the world market. With the integration of R&D and commercial production in a single building, DPI will cascade photomask production breakthroughs to its manufacturing sites throughout the world, thereby shortening the design-to-mask-to-wafer production cycle time.

AMD, DPI, and Infineon expect great technology synergies and competitive advantages by integrating the Mask Technology Center (AMTC and DuPont Photomasks Dresden) into their supply chains[1]. The Mask Technology Center is located in the vicinity of AMD´s Fab 30 and Fab36 (which is currently under construction) and Infineon´s 200 mm and 300 mm production and development sites in Dresden. The advantages of having a photomask R&D center and a commercial production facility housed in the same building and in the immediate proximity of industry leading fabs is self-evident: it means the shortest possible distance between development and production so that direct feedback between mask and wafer fabs is possible, which is important to the global semiconductor industry success.

2. RESEARCH ACTIVITIES

The AMTC has three R&D thrust areas or streams:

- Stream 1: Enhancement of existing mask technology through new processes and materials.
- Stream 2: Transfer of wafer R&D/manufacturing processes and methods to mask R&D/manufacturing.
- Stream 3: Development of new mask technologies for sub-70nm technologies (e.g., EUV).

All 3 streams require close cooperation with the AMTC's customers, partners, and suppliers. Stream 1 is executed at the AMTC in close cooperation with DPI's R&D network. Stream 2 is mostly driven through the cooperation with the AMTC partners' chip production and R&D sites in Dresden (Figures 2 and 3). Stream 3 is driven through the AMTC's R&D network. The AMTC is involved in many national and international mask technology research projects. For example, major activities on current and future mask processing technologies are conducted in the framework of a project, funded by the German Government, with 22 partners from industry and public research institutions. Development of both e-beam and laser mask writer technologies and processes, along with their corresponding data preparation activities, is performed with funds from the Saxony government. In addition, the AMTC is involved in cooperative European research activities on EUV and 157 nm mask development and handling.

2.1. Stream 1: Enhancement of existing mask technology

The R&D activities in this thrust area are focused on incoming blanks inspection, e-beam lithography, metrology, inspection and repair (see Figure 3). Examples are given below.

Decreasing feature sizes require more accurate and precise metrology, an example of which is the emerging need for 3-dimensional mask feature characterization. Besides photon and electron optical CD measurement, the AMTC employs AFM-based metrology techniques. The correlation of measurement results across metrology platforms is a challenge for advanced photomask development. Detailed work in this field has been performed at the AMTC and has been shown recently[2].

Recently, nano-machining mask repair technology has received much attention. The AMTC is evaluating this new technology as a beta partner and has demonstrated the ability to repair heretofore irreparable defects on 70 nm design

rule tritone masks by combining nano-machining with FIB repair. Figure 4 shows representative structures before and after repair. Ten programmed edge defects can now be repaired and cleaned (with CO_2 "snow") in 120 minutes. This repair time is 20-30% of that previously attainable with nano-machining and is comparable to FIB repair time.

Pellicle-induced photomask distortion, which is caused by a combination of aluminum frame warp and adhesive mechanical compliance limitations, results in image placement error. The 2003 ITRS sets the 65 nm node post-correction photomask image placement error budget at 15 nm. Figure 5 shows simulations of placement error for pellicle assemblies from AMTC's various pellicle suppliers. The calculated pre-compensation maximum placement distortion before compensation is shown in figure 5b.

2.2. Stream 2: Transfer of wafer R&D/manufacturing processes and methods to mask R&D/manufacturing

One mask manufacturing process module that has benefited from the experience of semiconductor manufacturing is dry etch, specifically the adaptation of 300 mm wafer etch technology to photomask etching. Compared to previous designs, the chamber employed at AMTC has less moving parts, radially adjustable plasma density, increased pumping speed (2000 l/min.), and modified gas flow. This chamber technology produces excellent etch results on MoSi-based phase shifting masks. The data in Figure 6 show that phase shift targeting is stable at ~180º, and the phase shift nonuniformity is less than 2º.

Another area benefiting from the combined experience of mask and wafer manufacturers is physical plant design and management. The AMTC cleanroom is class 100 with fully integrated SMIF-based mini-environments, ensuring contamination-free mask handling with attractive cleanroom costs. The capital cost savings is about 1000€/m², while the electricity cost savings is about 260 €/m²/year.

To insure that the required cleanliness level is obtained and kept throughout the mask production process an extensive monitoring process was set up which closely follows ideas developed for wafer fabs[6].

2.3. Stream 3: Development of mask technologies for sub-70nm lithography (including EUV)

Until recently, 157 nm lithography received high priority for 65 and 45 nm design rules, so the AMTC and its partners pursued it agressively. However, due to the recent emphasis on 193 nm immersion lithography, 157 nm activities will receive low priority in the future. Here we present two examples of work performed on 157 nm lithography issues. First, over the past several years, International SEMATECH, in cooperation with Infineon/AMTC-Dresden and SELETE, funded a joint development project with Carl Zeiss to develop a 157 nm AIMS™ tool. In 2003, three tools were shipped to the three beta customer sites. Initial results were recently published[3].

Secondly, the hard pellicle, which circumvents the soft pellicle radiation durability problem, introduces an additional optical element into the 157 nm exposure tool, resulting in refraction-induced feature shift on the wafer (see Figure 7). The usual correction scheme applied in the scanner compensates for most of the induced distortion; residual distortion is about 3 nm on the wafer. With pellicle pre-shaping, the effect can be reduced to less than 1 nm on the wafer.

The AMTC is developing new handling methods, materials, processes, and characterization methods for EUV photomasks. Examples of this work are shown below.

The effect of chucking on EUV mask flatness must be understood to ensure a adequate placement accuracy during wafer exposure. Calculations show that the mask flatness specified for the EUV mask and chuck in the worst case depicted in figure 8 does not lead to the desired 50 nm peak-to-valley composite flatness. Assuming a 50 nm mask warp and a similar chuck warp, calculations show that the composite flatness in the mask quality area will be above 87 nm. The induced in-plane distortion for the 6º incidence angle will be >1 nm.

EUV etch study test masks described below were processed by the AMTC's partner IMS Chips in Stuttgart and have been presented in detail elsewhere[4]. The masks contain a variety of features. Figure 9 shows SEM cross-sections of dense lines and contact holes in the absorber with a nominal mask-level CD of 125 nm for different absorber materials. This corresponds to the feature size required for the 32 nm node. The chrome absorber benchmark was etched with a standard Cr process in a Cl/O_2 atmosphere. TaN-based materials were etched in pure Cl.

The Cr absorber shown in Figure 9a with a 50% overetch time shows approximately a 1:1 pitch for dense lines. However, the layer is not fully etched, and footing is clearly visible. With 100% overetch time, the footing is removed and straight side walls result, but the linewidth is considerably reduced by the isotropic etch component and equal lines and spaces cannot be obtained. This effect is even more pronounced for contact holes with the same CD if they are etched simultaneously with the lines. Contact holes require more overetch time than dense lines for a comparable etch profile. The optimum overetch time also depends on the feature size (the well-known RIE lag effect).

Etch results for two different TaN-based EUV absorbers are shown in Figures 9b and 9c. Neither TaN-based material exhibits much CD sensitivity to overetch time for dense lines or contact holes, and no footing is observed. One of the materials shows sidewall bowing. The etch processes for both TaN absorbers are still preliminary and can be improved. These results demonstrate the potential of TaN for an EUV absorber.

The EUV mask must exhibit a uniform and high reflectivity for optimum printing performance. Mask processing can reduce the reflectance below that of the incoming blank. Critical process issues include Si capping layer oxidation, heating, and ion bombardment. The current process reduces reflectance by ~3% absolute and has little effect on nonuniformity. Figure 10 is a reflectance uniformity plot, showing a 0.3% maximum deviation, sufficient to meet the 32 nm ITRS requirements.

3. SUMMARY

This paper provided an overview of a few of the R&D activities at the Advanced Mask Technology Center Dresden. The combination of R&D partnering and best practice technology sharing is critical to maximize semiconductor device performance. The R&D collaboration and commercial photomask production between the AMTC and DuPont Photomasks Dresden enable AMD, DuPont Photomasks, and Infineon to achieve technology leadership and drive the much-needed innovations for sub-70nm technologies.

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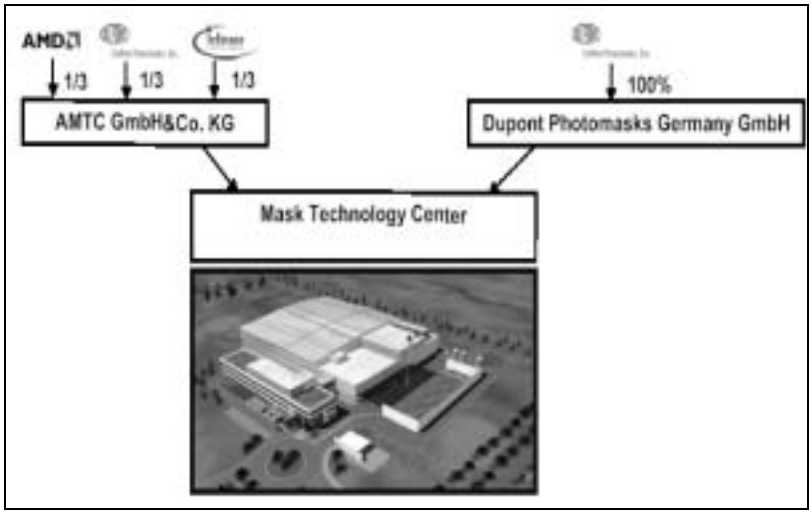


Figure 1. The AMTC is located in the Mask Technology Center Dresden alongside a state-of-the-art commercial mask production facility operated by DuPont Photomasks. The AMTC focuses on photomask R&D and pilot production, while DuPont Photomasks-Dresden focuses on the production of commercially-available advanced photomasks. Close cooperation ensures full service to the customer (e.g. pilot samples from AMTC and production mask sets from DuPont Photomasks-Dresden).

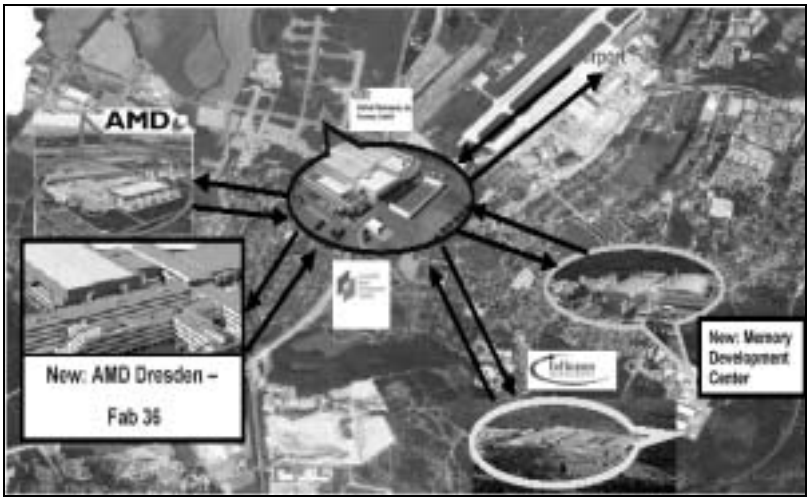
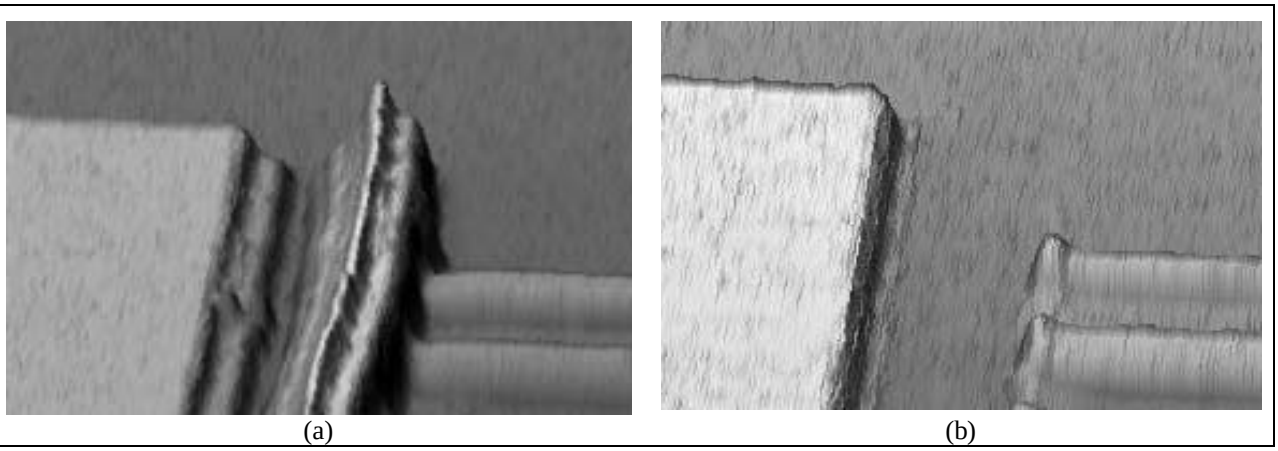


Figure 2. The AMTC is located close to the most advanced chip manufacturing sites of its partners in Dresden. This enables close cooperation between the partners. The AMTC will benefit from the close cooperation with its partners, in particular in the fields with a strong leadership of chip technology versus mask technology (see also Figure 3).

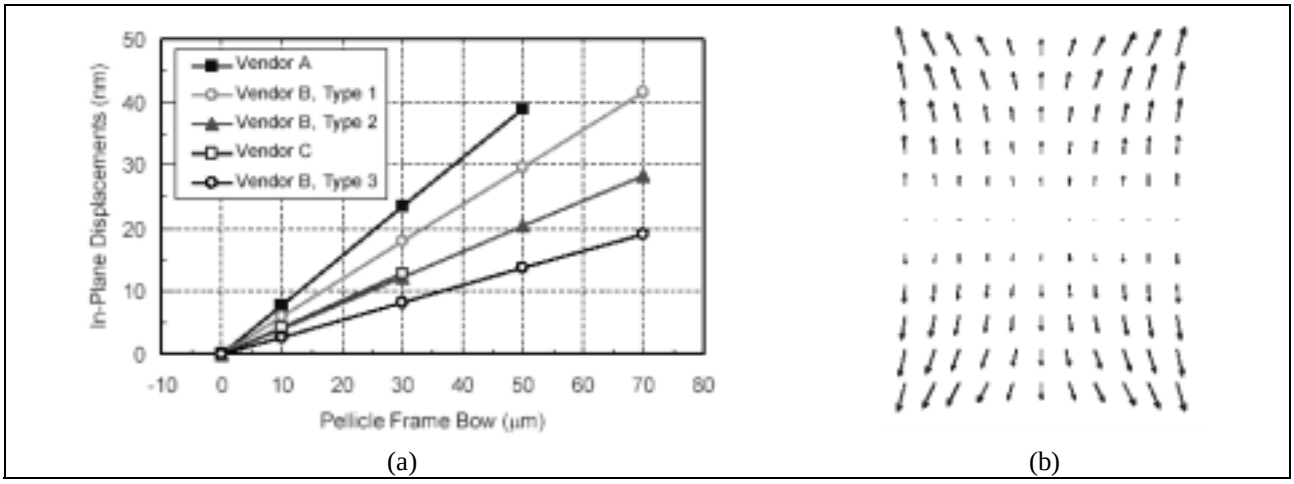
Main Processes:	
Data Preparation	Low
Coating	High
Ebeam Lithography	Low
DUV Lithography	High (green)
Resist Process	High
Dry Etch	High
Resist Strip / Resist Cleaning	High
Yield Mgt	High
CD Metrology	High
Overlay Metrology	Low (blue)
Inspection	Medium (yellow)
Repair	Low
Pellicle Mount	Low
Support Process:	
Facility Mgt	High
Material Mgt	High
IT/IS	High
Production Control	Medium

Figure 3. The table shows an overview of key module development and support process areas. In many areas, the synergies between chip production / R&D and mask production / R&D are very high. The use of these synergies will be a key stream of the AMTC's research.



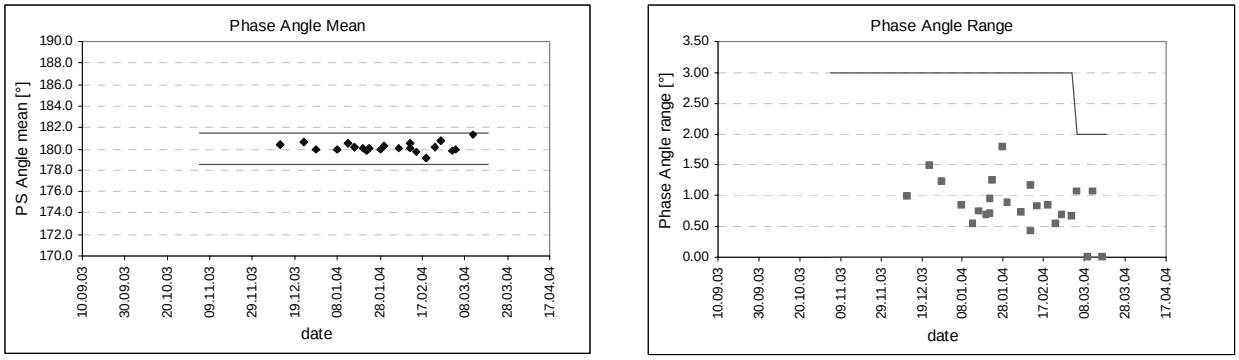
(a) (b)

Figure 4. The figures shows a successful repair of a dark "killer" defect with the new RAVE nm650 nano-machining tool. The defect extends over almost 8 µm in tight structures on a 70 nm customer tritone mask. (a): before repair. (b): after the nano machining process. Note also that the structure was brought into spec by additional FIB depositions.



(a) (b)

Figure 5. (a) Finite element simulation results showing placement error for frames and adhesives from AMTC's various pellicle vendors. (b) A vector plot showing typical in-plane distortion created by mounting the pellicle to the photomask.



(a) (b)

Figure 6. The Phase Angle mean (a) and uniformity range (b) of the MoSi dry etch process on an AMAT Tetra 2 etcher, measured over an area covering 130x130 mm (measured on a test plate at 9 locations).

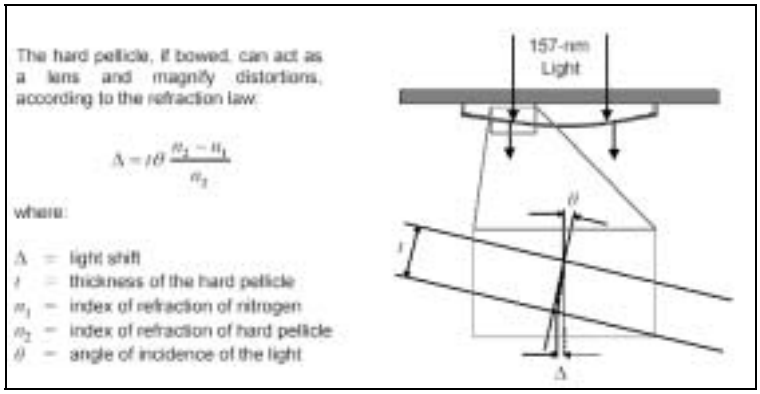


Figure 7. The figure shows how a bowed hard pellicle for 157 nm lithography can act as a lens and generate pattern placement error.

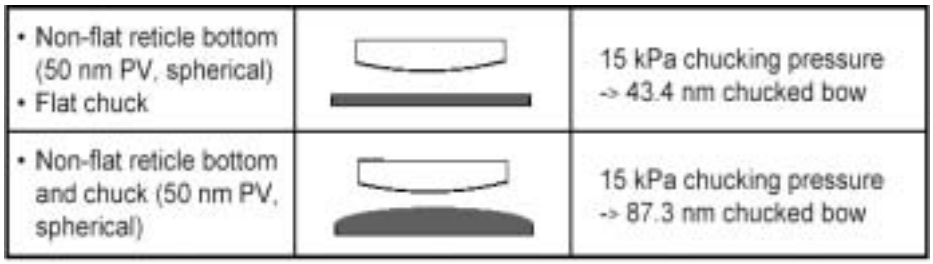


Figure 8. In the worst case, even when both the EUV blank and the chuck meet flatness specs, the complete system with the mask chucked at a pressure of 15 kPa no longer gives the desired overall flatness in the quality area.

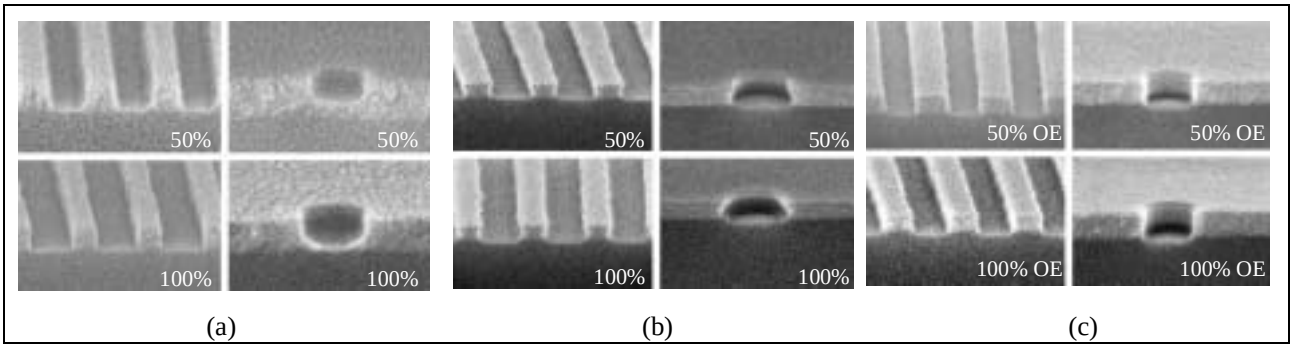


Figure 9. Results of EUV absorber etch tests performed at the IMS Stuttgart. Shown are the cross sections of 125 nm dense lines and contact holes for Cr absorber (a) and two different TaN absorbers (b and c). 50% and 100% overetch cases are shown. Cr etch behavior varies with over-etch time for both contact holes and dense lines and includes a considerable etch bias. The two TaN materials have different sidewall profiles, but both are relatively insensitive to over-etch time and show almost no etch bias.

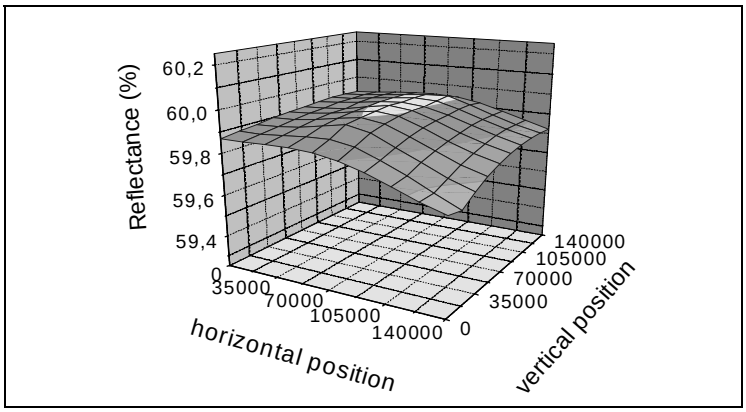


Figure 10. This figure shows the reflectance across the quality area of a patterned EUV mask. The measurements were performed at the synchrotron radiation beamline of the PTB at BESSY II and show a reflectance uniformity across the plate of less than 0.3%, which already fulfills the ITRS requirements.